ABSTRACT OF THE DISCLOSURE

A method for testing memories has steps of providing seamless data to data input/output pins and providing seamless control commands to each bank at each clock cycle, when the memories receive the seamless data and control commands, and the data input/output pins of memories receive heavy loads status. For SDRAM and DDR-DRAM, control commands and data are seamlessly inputted/outputted at each clock cycle. For RDRAM, control commands are inputted at each "command packet", whereby data are inputted/outputted at each "data packet" and memories are in the heavy loading status. By providing heavy loading to control pins and data input/output pins of memories, it is easy to detect weakened memories.